

[CLAIMS]

We claim:

- 1 1. An integrated circuit chip comprising:
2 an array of pads, said pads including signal I/O, power and power
3 return pads;
4 a plurality of I/O cells each being connected to one of said I/O pads by
5 I/O signal wiring in one or more wiring layers; and
6 a plurality of ESD protection devices, each of said plurality of ESD
7 protection devices being connected to one of said array of pads by a metal
8 line, said metal line meeting an ESD width constraint and having a resistance
9 below an ESD resistance constraint.

- 1 2. The integrated circuit chip of Claim 1, wherein the plurality of ESD
2 protection devices comprises:
3 an ESD protect device in each of said plurality of I/O cells connected
4 between an I/O circuit in said I/O cell and one of said I/O signal pads.

- 1 3. The integrated circuit of claim 2 wherein each said ESD protect device
2 is further connected to power rails and power return rails connected to said
3 circuit.

- 1 4. The integrated circuit chip of claim 3, wherein the plurality of ESD
2 protection devices comprises:
3 an ESDxx cell connected between power rails and power return rails
4 for at least two different power supplies.

1 5. The integrated circuit chip of claim 4 further comprising:
 2 a plurality of ESDxx cells, each of said plurality of ESDxx cells being
 3 associated with a group of I/O cells.

1 6. The integrated circuit chip of claim 5 further comprising:
 2 a plurality of said I/O signal lines being designated as unused, said
 3 unused I/O signal lines being connected to one of said power or power return
 4 rails.

1 7. A chip design method comprising the steps of:
 2 a) retrieving a wire width constraint from technology data for an
 3 I/O cell;
 4 b) retrieving a maximum resistance constraint from said
 5 technology data for said I/O cell;
 6 c) propagating said wiring width constraint and said maximum
 7 resistance constraint to net design data for said chip;
 8 d) generating said chip, connections between said I/O cell and an
 9 associated pad being constrained by said propagated constraints; and,
 10 e) checking said wired integrated circuit.

1 8. The method of claim 7, wherein a plurality of I/O cells are wired and
 2 further comprising before the checking step (e), repeating steps (a) - (d) for
 3 each of said plurality of I/O cells.

1 9. The method of claim 8, further comprising before the checking step
2 (e), the step of:

3 d1) wiring any unused chip pads to a cell including a connection to
4 power rail or to a power return rail.

1 10. The method of claim 8, further comprising before the checking step
2 (e), the step of:

3 d1) wiring any unused chip pads to a cell including an ESD protect
4 device.

1 11. The method of claim 8, wherein the generating step (d) comprises the
2 step of:

3 i) placing each of said I/O cells based on said propagated wire
4 width and maximum resistance constraints; and

5 ii) routing a connection between each said placed I/O cell and its
6 said associated pad, each said routed connection meeting said propagated wire
7 width and maximum resistance constraints.

1 12. The method of claim 11, wherein the checking step (e) comprises
2 checking connections made in said generating step (d) against propagated wire
3 width and maximum resistance constraints.

1 13. A chip design method comprising the steps of:

2 a) retrieving a power route pattern instruction;

3 b) identifying power and power return connections;

4 c) routing each said power and each said power return connection,
5 each said routed connection meeting wire width and maximum resistance
6 constraints in said retrieved power route pattern instruction; and

7 d) checking said wired integrated circuit.

1 14. The method of claim 13, wherein the routing step (c) includes
2 identifying any unused chip pads and wiring said unused pad to a power rail
3 or to a power return rail.

1 15. The method of claim 13, wherein the routing step (c) includes
2 identifying any unused chip pads and wiring said unused pad to a cell
3 including an ESD protect device.

1 16. The method of claim 13, wherein the routing step (c) includes the steps
2 of:

3 i) providing an ESDxx cell; and

4 ii) connecting said ESDxx cell between power rails and power
5 return rails for at least two different power supplies.

1 17. A chip design method comprising the steps of:

2 a) retrieving I/O and ESDxx cell identifications and placement
3 constraints;

4 b) providing a plurality of ESDxx cells for placement;

5 c) placing each of said plurality of ESDxx cells with a group of
6 I/O cells;

7 d) connecting each said placed ESDxx cell between power rails
8 and power return rails for at least two different power supplies; and,

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